CLAIMS

What is claimed is:

1. A system configured to interact with a virtual bus interface that produces a bus-type transaction from a point-to-point type transaction, the system comprising:

a detection logic operably connectable to the virtual bus interface, the detection logic being configured to detect a cache coherence protocol mode associated with an originating system that provides the point-to-point type transaction to be processed by the virtual bus interface; and

a coding logic operably connectable to the detection logic and the virtual bus interface, the coding logic being configured to control how a cache coherence transaction received from the originating system is processed by the virtual bus interface based, at least in part, on the cache coherence protocol mode detected by the detection logic.

2. The system of claim 1, where the detection logic is configured to determine the cache coherence protocol mode by referencing a state machine configured to track transaction types encountered in a set of cache coherence transactions.

3. The system of claim 1, where the detection logic is configured to determine the cache coherence protocol mode by determining whether a first transaction type initiated by a processor in the originating system is responded to with a second transaction type from a memory controller in the originating system.

4. The system of claim 3, where the first transaction type comprises a processor-initiated self-snoop request and the second transaction type comprises a memory agent initiated self-snoop request.

5. The system of claim 3, where the first transaction type comprises a data read transaction and the second transaction type comprises a data invalid transaction.

6. The system of claim 1, the detection logic being configured to initially assume that the cache coherence protocol mode is a directory-based protocol.

7. The system of claim 6, the coding logic being configured to treat a port read line code self snoop (PRLCSS) request as a port read line code (PRLC) request until the detection logic determines that the cache coherency protocol mode is a snooping protocol.

8. The system of claim 7, where the detection logic determines that the cache coherence protocol mode is a snooping protocol by determining that a port read line code self snoop request (PRLCSS) initiated by a processor is responded to by a self snoop request from a simple memory agent.

9. The system of claim 8, where upon the detection logic determining that the cache coherence protocol mode is a snooping protocol, the coding logic is dynamically reconfigured to treat the port read line code self snoop (PRLCSS) request previously treated as a port read line code (PRLC) request as a port read line code self snoop (PRLCSS) request.

10. A virtual bus interface system configured to produce a bus-type transaction from a point-to-point type transaction, comprising:

a point-to-point transaction logic configured to receive a packet associated with a point-to-point transaction from a point-to-point linked system;

a detection logic configured to detect a cache coherence protocol mode associated with the point-to-point linked system by examining a set of packets associated with the point-to-point type transaction;

a bus-type transaction logic configured to selectively produce a bus-type transaction from a point-to-point transaction received by the point-to-point transaction logic; and

a coding logic configured to control how a transaction received from the point-to-point linked system is processed by the bus-type transaction logic based, at least in part, on the cache coherence protocol mode detected by the detection logic.

11. The system of claim 10, where the detection logic is configured to reference a state machine that is configured to track transaction types encountered in a set of cache coherence transactions and to determine whether a first transaction type initiated by a processor in the originating system is responded to with a second transaction type from a memory controller.

12. The system of claim 11, where the first transaction type comprises a processor initiated self-snoop request and the second transaction type comprises a simple memory agent initiated self-snoop request.

13. The system of claim 12, the detection logic being configured to initially assume that the cache coherence protocol mode is a directory-based protocol.

14. The system of claim 13, the coding logic being configured to treat a port read line code self snoop (PRLCSS) request as a port read line code (PRLC) request until the detection logic determines that the cache coherency protocol mode is a snooping protocol, and upon the detection logic determining that the cache coherence protocol mode is a snooping protocol by determining that a port read line code self snoop request (PRLCSS) initiated by a processor is responded to by a self snoop request from a simple memory agent treating the port read line code self snoop (PRLCSS) request previously treated as a port read line code (PRLC) request as a port read line code self snoop (PRLCSS) request.

15. A method, comprising:

setting a cache coherence protocol mode to a directory mode;

detecting a completion event associated with a point-to-point transaction being received in a virtual bus interface;

determining the cache coherency protocol mode associated with a system producing the point-to-point transaction by examining a set of packets associated with the point-to-point transaction; and

selectively processing a packet associated with the point-to-point transaction into a bus-type transaction based, at least in part, on the cache coherency protocol determined.

16. The method of claim 15, where determining the cache coherency protocol mode includes:

establishing a first state in response to receiving a first packet associated with the point-to-point transaction;

selectively establishing a second state in response to receiving a second packet associated with the point-to-point transaction, where the second packet is generated by the system producing the point-to-point transaction in response to the first packet; and

selectively resetting the cache coherence protocol mode to snooping mode based, at least in part, on the second state.

17. A computer-readable medium storing processor executable instructions operable to perform a method, the method comprising:

setting a cache coherency protocol mode to a directory mode;

detecting a completion event associated with a point-to-point transaction being received in a virtual bus interface;

determining the cache coherency protocol mode associated with the system producing the point-to-point transaction by:

establishing a first state in response to receiving a first packet associated with the point-to-point transaction;

selectively establishing a second state in response to receiving a second packet associated with the point-to-point transaction, where the second packet is generated by the system producing the point-to-point transaction in response to the first packet; and

selectively resetting the cache coherence protocol mode to a snooping mode based, at least in part, on the second state; and

selectively processing a packet associated with the point-to-point transaction into a bus-type transaction based, at least in part, on the cache coherency protocol detected.

18. A system, comprising:

means for receiving a packet associated with a point-to-point transaction;

means for detecting a cache coherency protocol mode based, at least in part, on the packet; and

means for selectively producing a bus-type transaction from the point-to-point transaction, where the producing is controlled, at least in part, by the cache coherency protocol mode detected.

19. A set of application programming interfaces embodied on a computer-readable medium for execution by a computer component in conjunction with detecting a coherency protocol mode in a virtual bus interface, comprising:

a first interface for communicating a point-to-point type packet;

a second interface for communicating a cache coherency protocol mode data; and

a third interface for communicating a bus-type packet selectively processed from the point-to-point packet, where the bus-type packet processing depends, at least in part, on the cache coherency protocol mode data.